

MS-7680 Ver:3.2 m-ATX : 245 X 210mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71889AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 UP1625 4+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT CPU SA

Controller:uP6103

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x8

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

LPT Header *1

on BOARD BUZZER

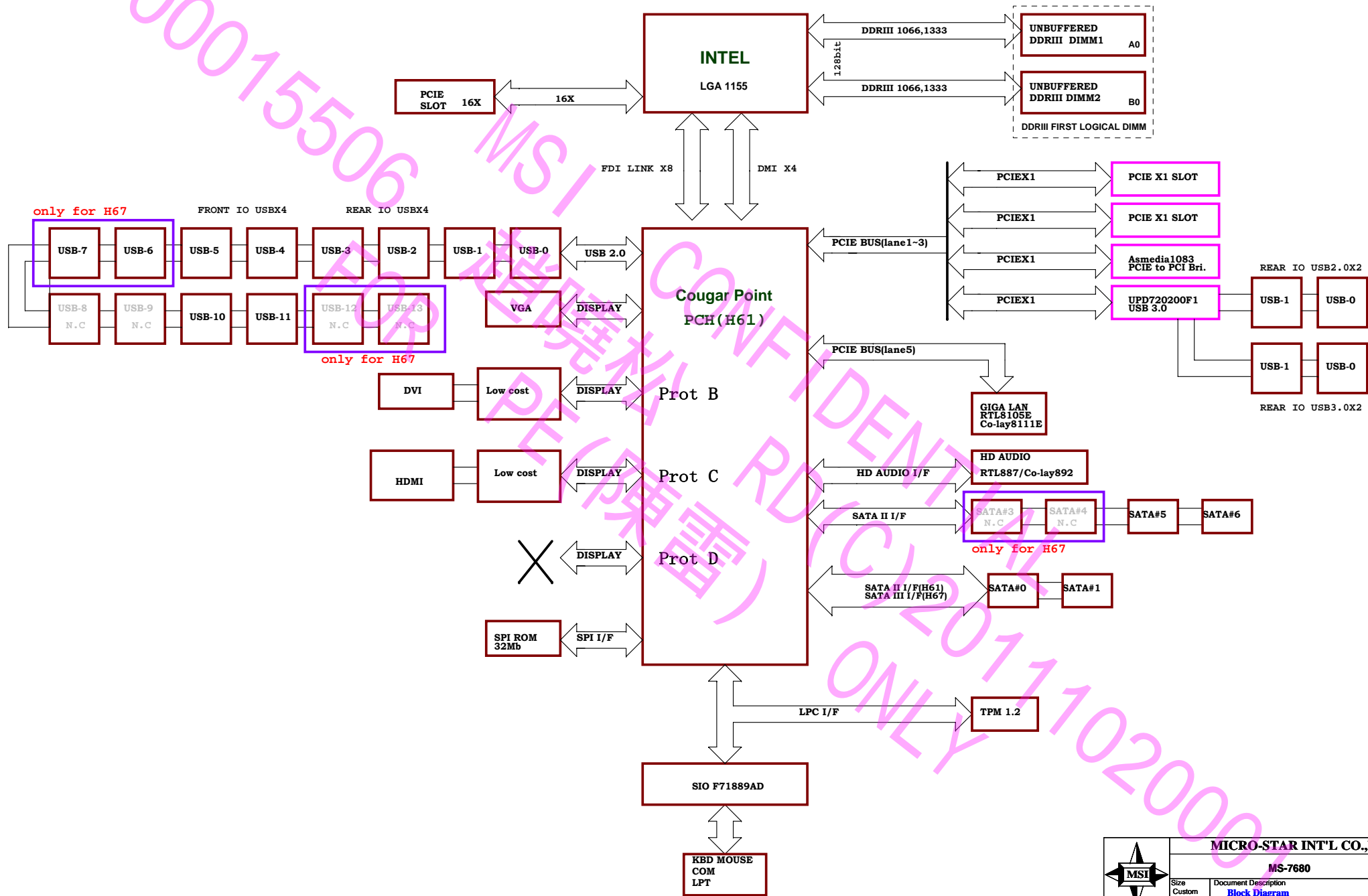
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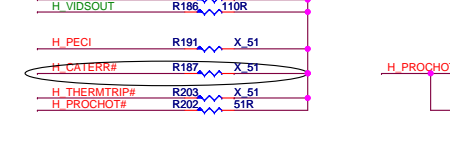
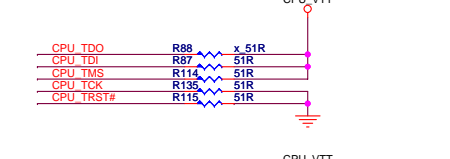
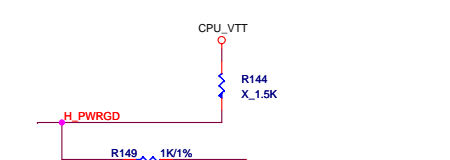
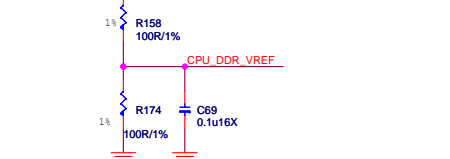
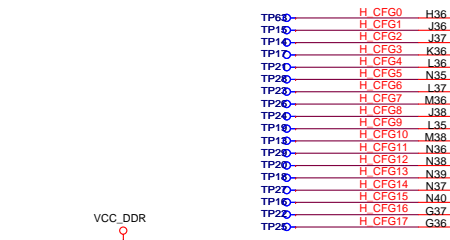
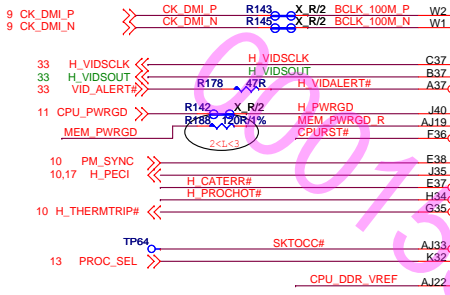


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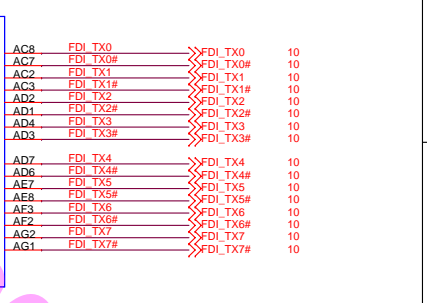
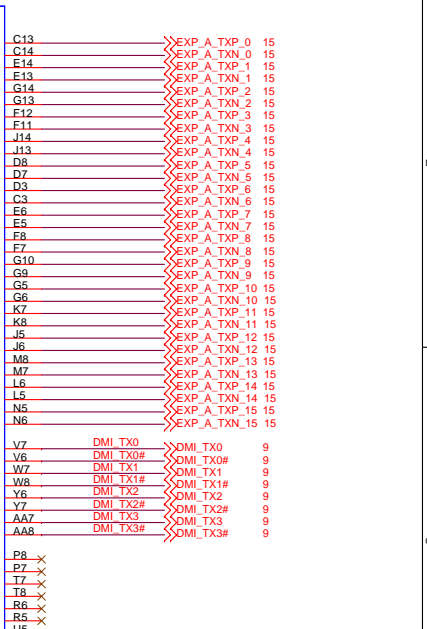
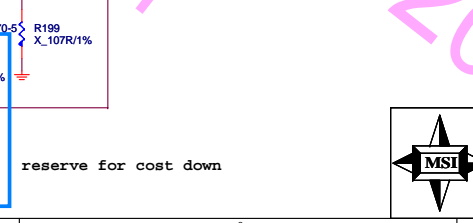
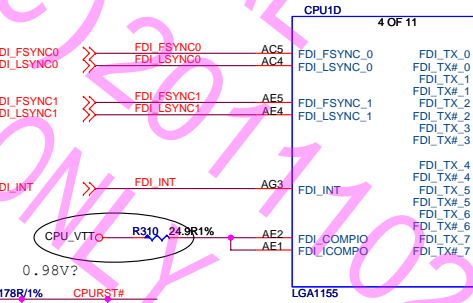
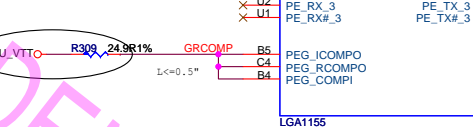
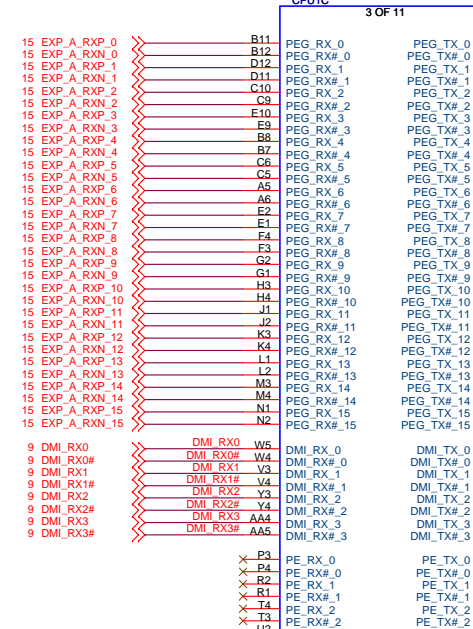
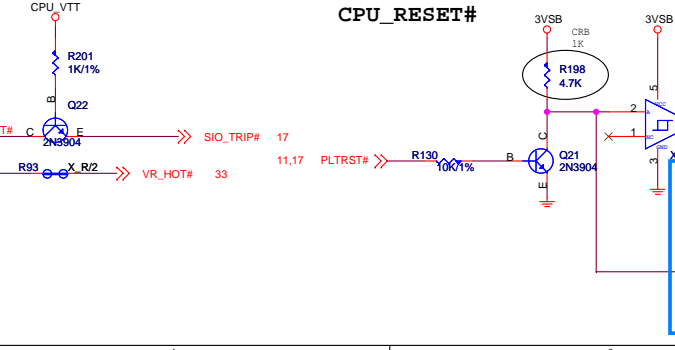
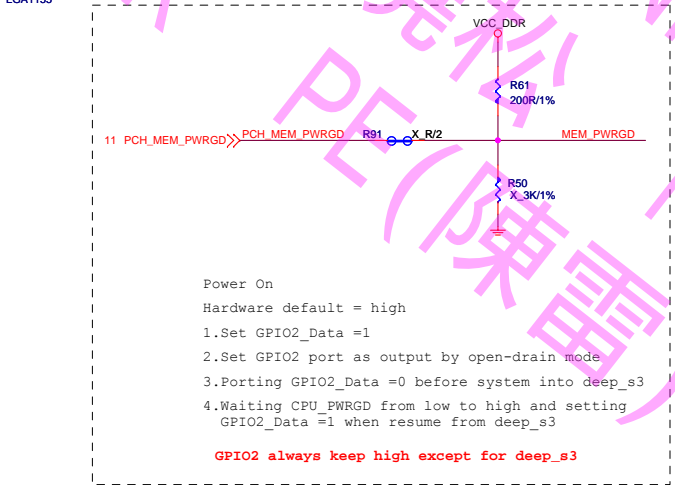
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PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

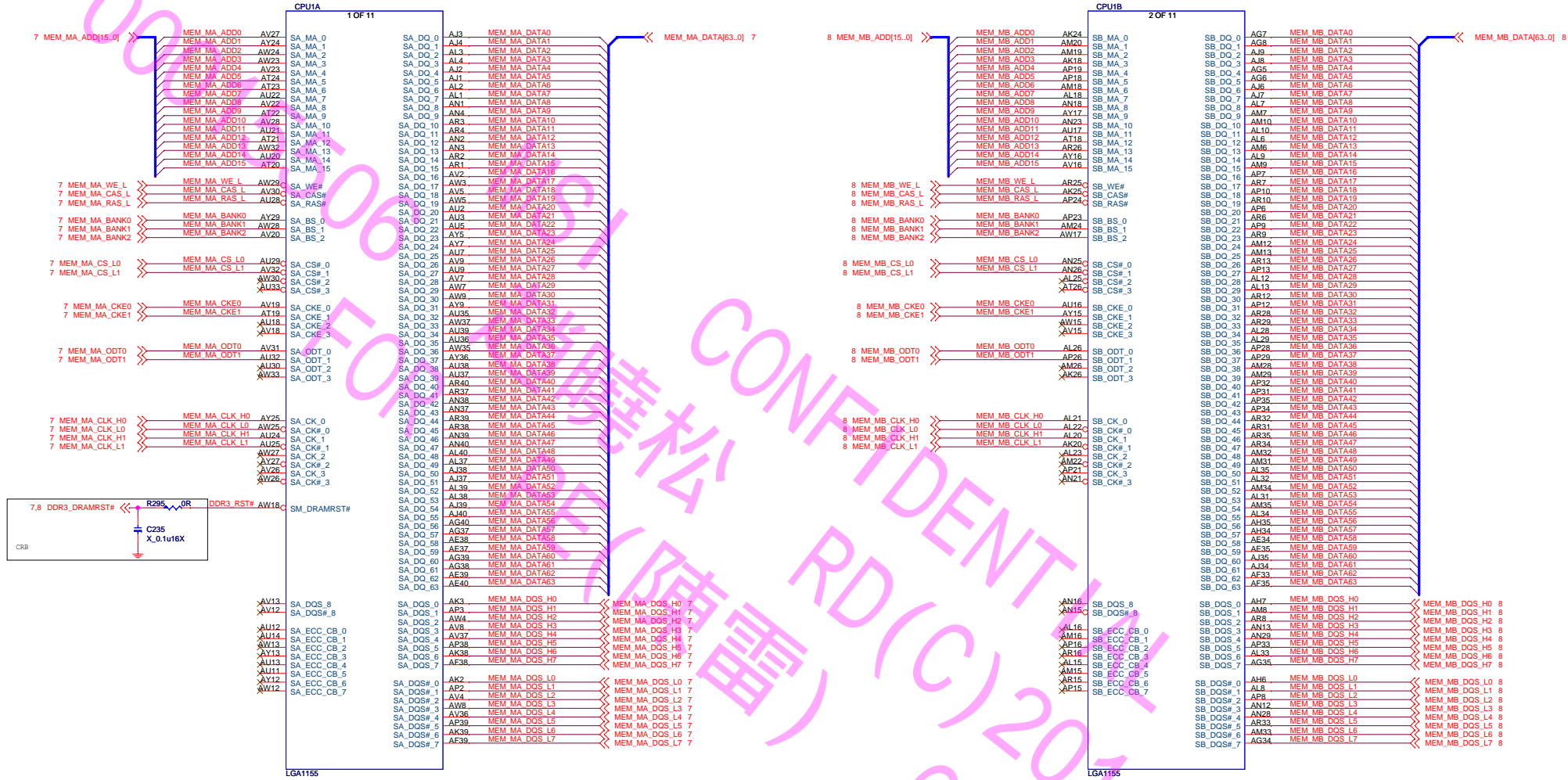


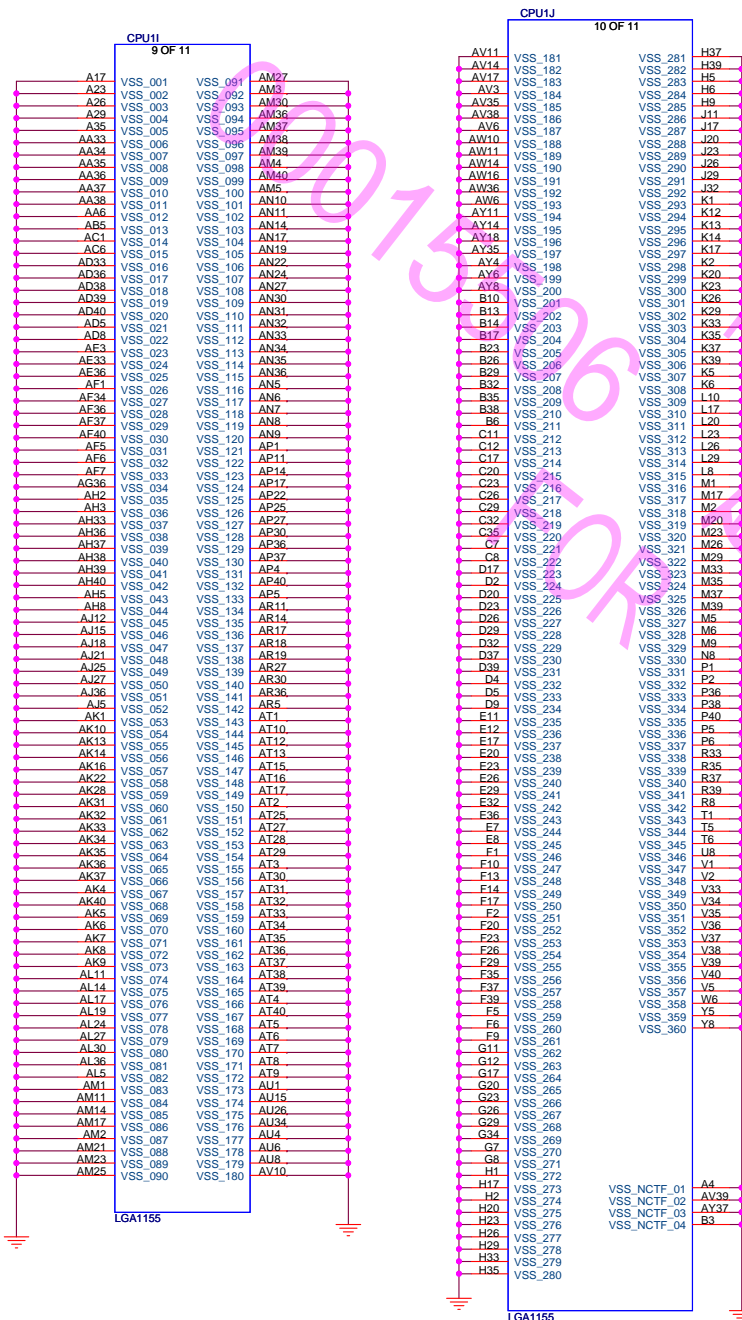
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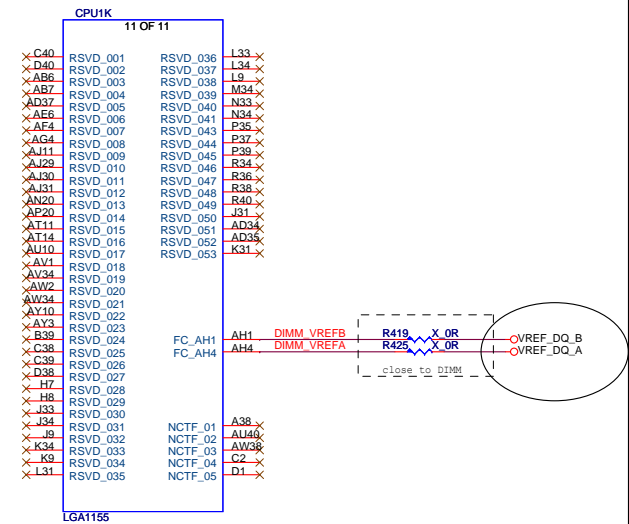
Size Custom Document Description **GPU-CLK/Control/MISC/PEG** Rev 3.2

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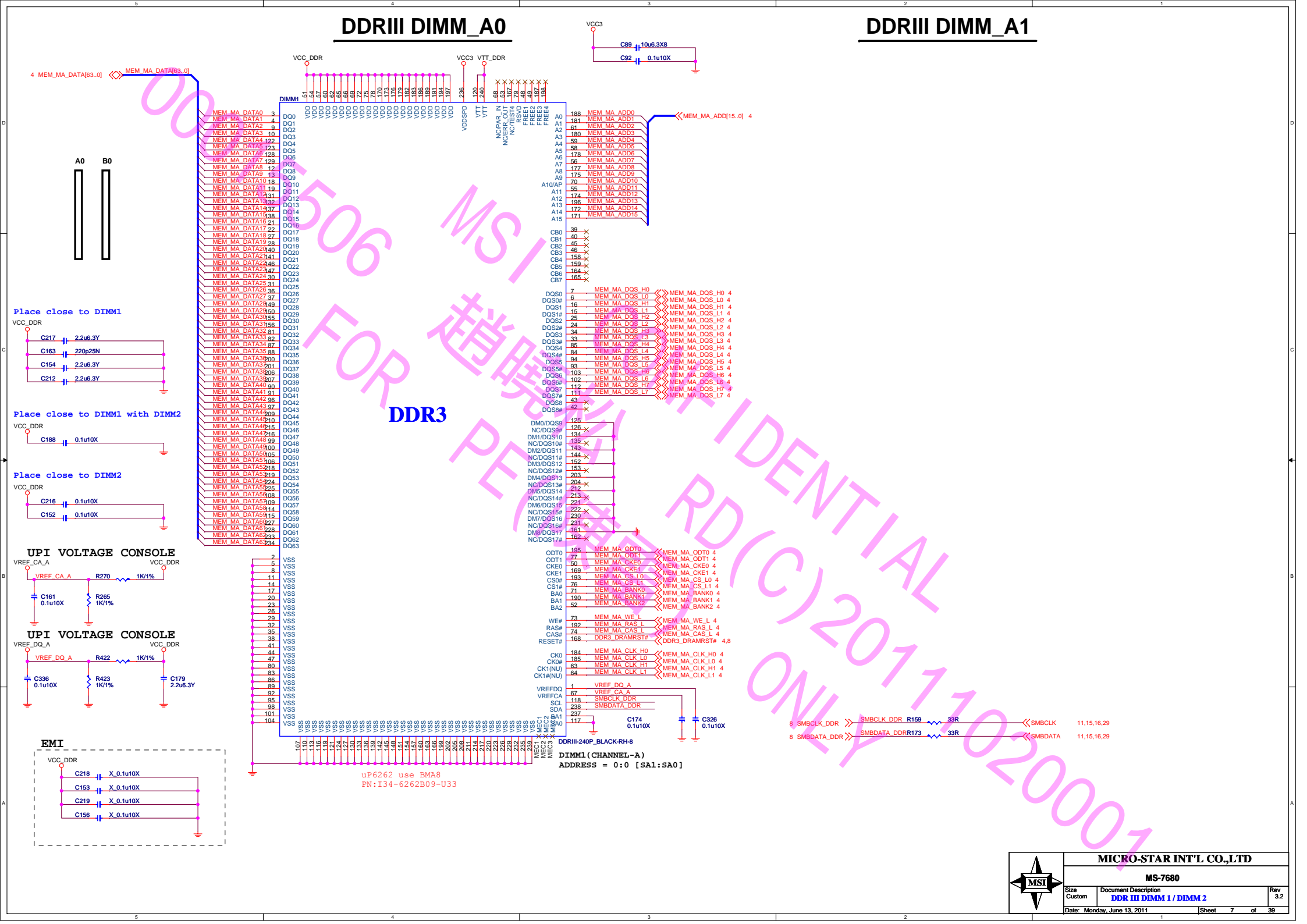


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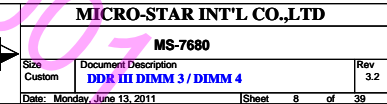


DDRIII DIMM_A0

DDRIII DIMM_A1

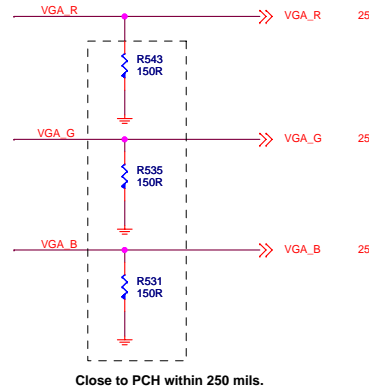
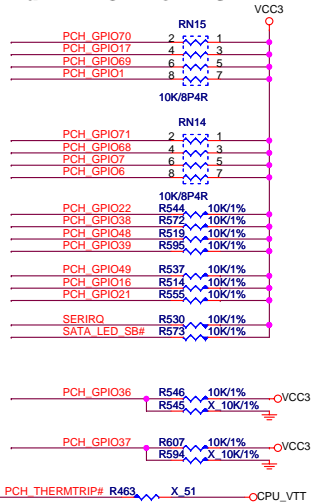


DDR3

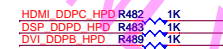




Pull HIGH for PCH



No VGA(pull down)



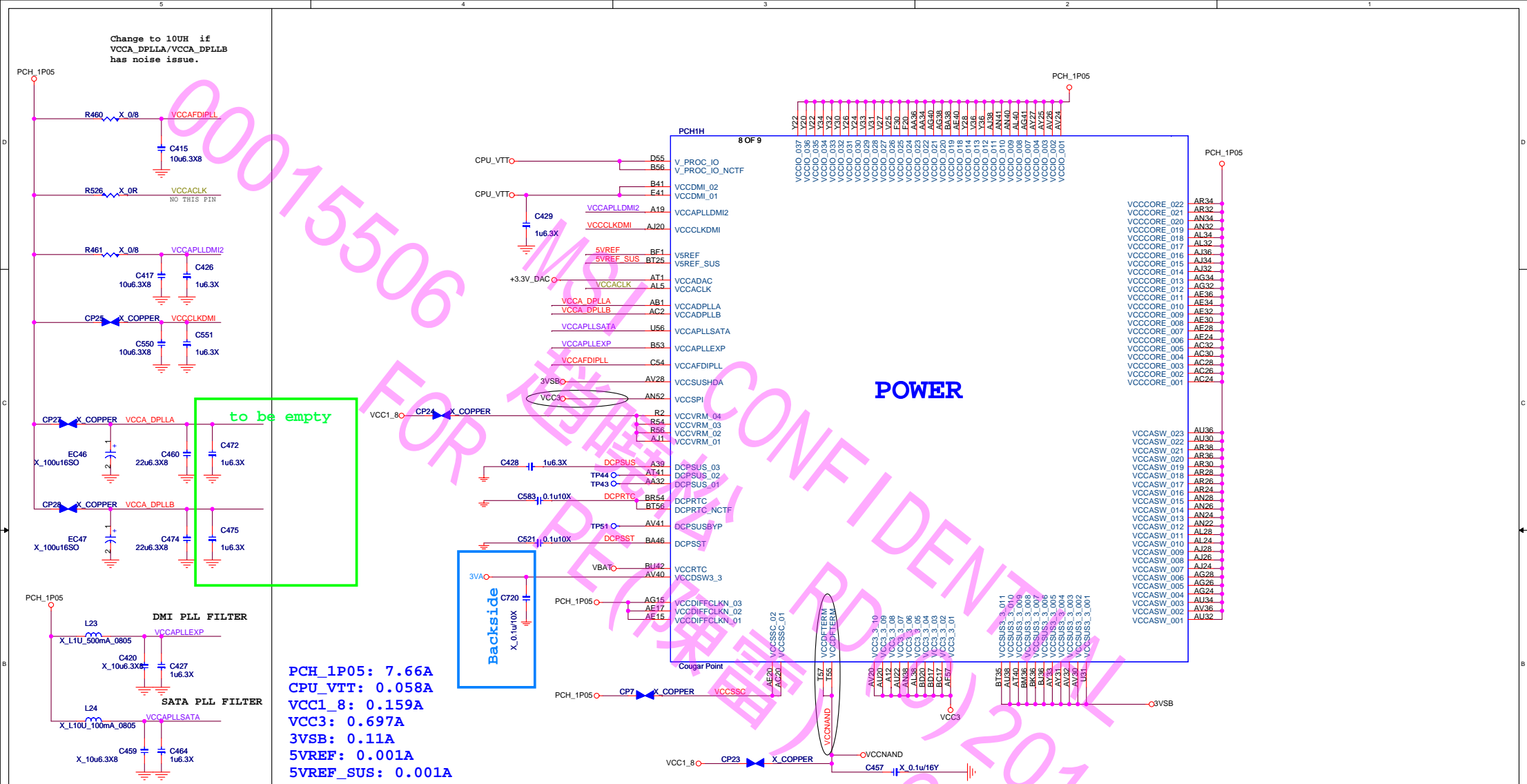
Enable VGA(CTRLCLK/DATA Pull High)

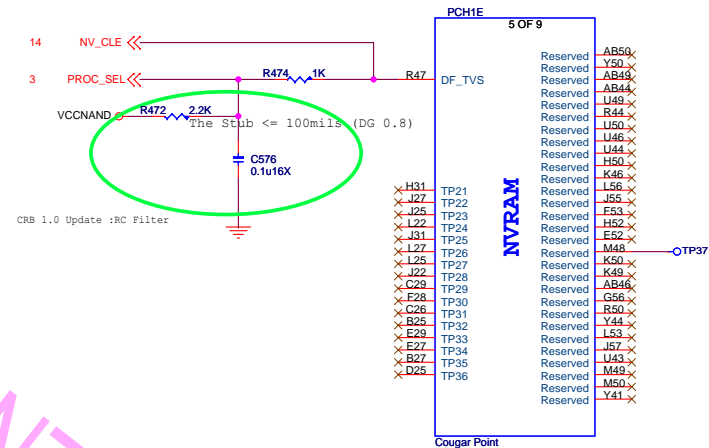
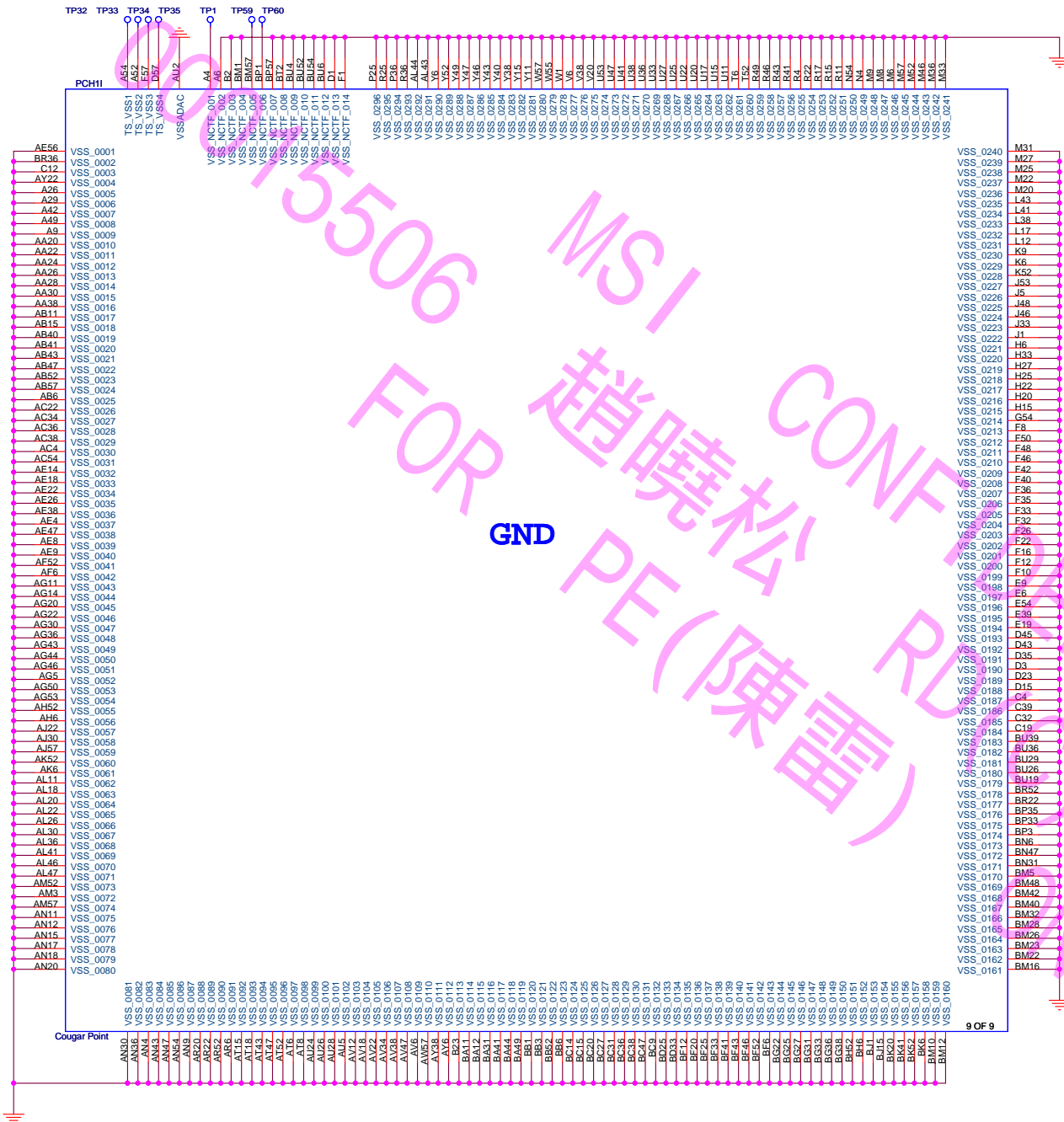


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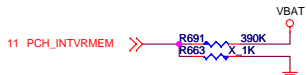
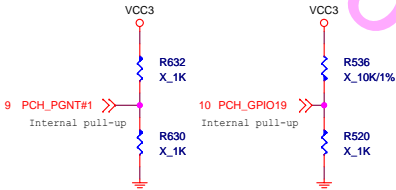
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



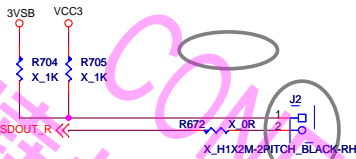
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



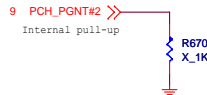
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

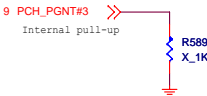


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

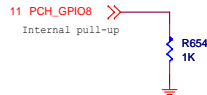
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



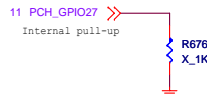
DMI AC/DC MODE
0 : AC
1 : DC *



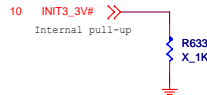
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

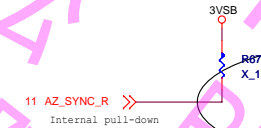


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INIT3_3V#
0 : ??????????????
1 : ?????????????? *

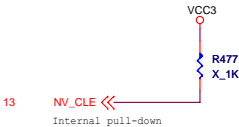
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



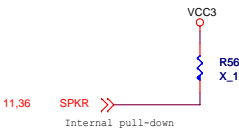
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



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PCI_Express X16 slot

PCI EXPRESS x1-PORT

Trace width > 200 mils

7,11,16,29 SMBCLK SMBCLK
7,11,16,29 SMBDATA SMBDATA

3VSB WAKE# WAKE#

3 EXP_A_TXP_0 EXP_A_TXN_0

3 EXP_A_TXP_1 EXP_A_TXN_1

3 EXP_A_TXP_2 EXP_A_TXN_2

3 EXP_A_TXP_3 EXP_A_TXN_3

3 EXP_A_TXP_4 EXP_A_TXN_4

3 EXP_A_TXP_5 EXP_A_TXN_5

3 EXP_A_TXP_6 EXP_A_TXN_6

3 EXP_A_TXP_7 EXP_A_TXN_7

3 EXP_A_TXP_8 EXP_A_TXN_8

3 EXP_A_TXP_9 EXP_A_TXN_9

3 EXP_A_TXP_10 EXP_A_TXN_10

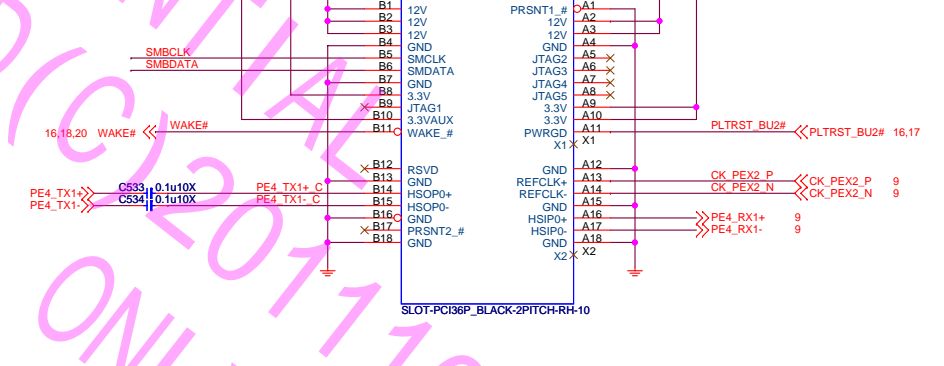
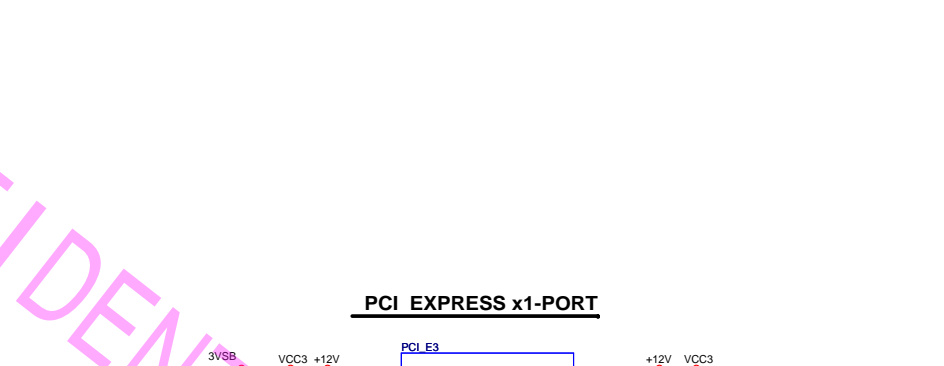
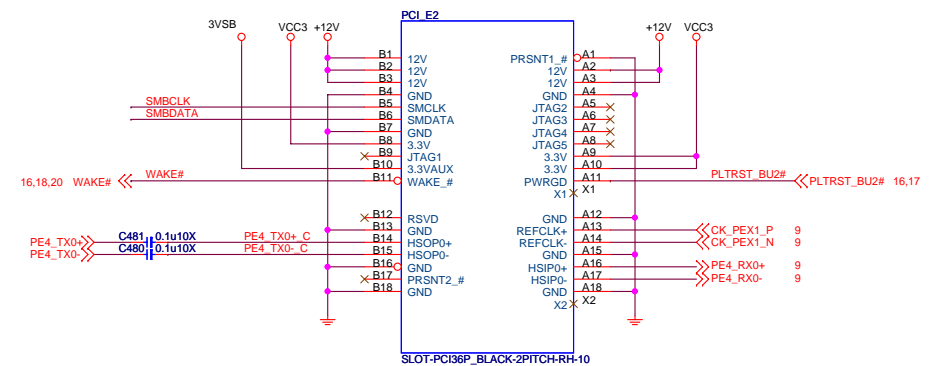
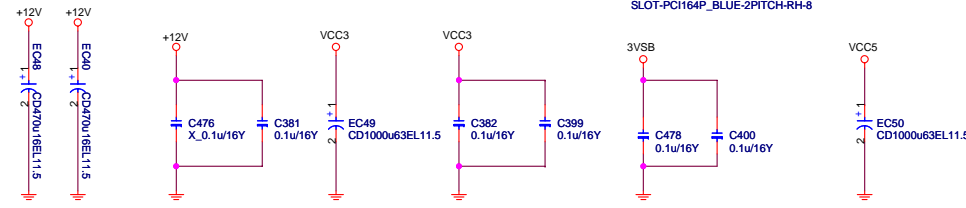
3 EXP_A_TXP_11 EXP_A_TXN_11

3 EXP_A_TXP_12 EXP_A_TXN_12

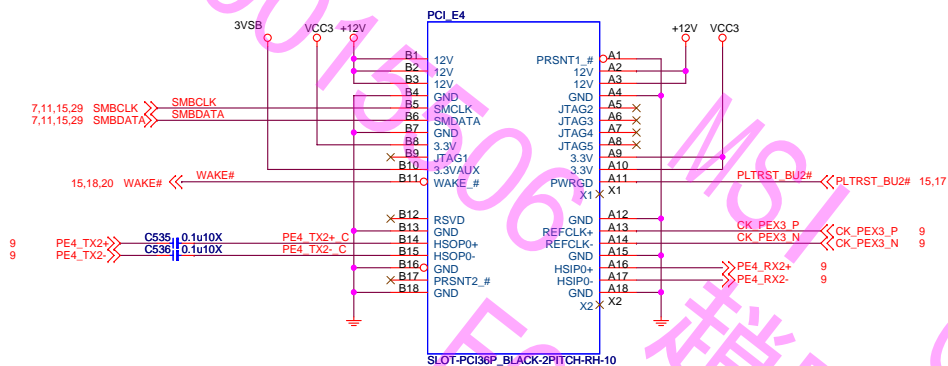
3 EXP_A_TXP_13 EXP_A_TXN_13

3 EXP_A_TXP_14 EXP_A_TXN_14

3 EXP_A_TXP_15 EXP_A_TXN_15



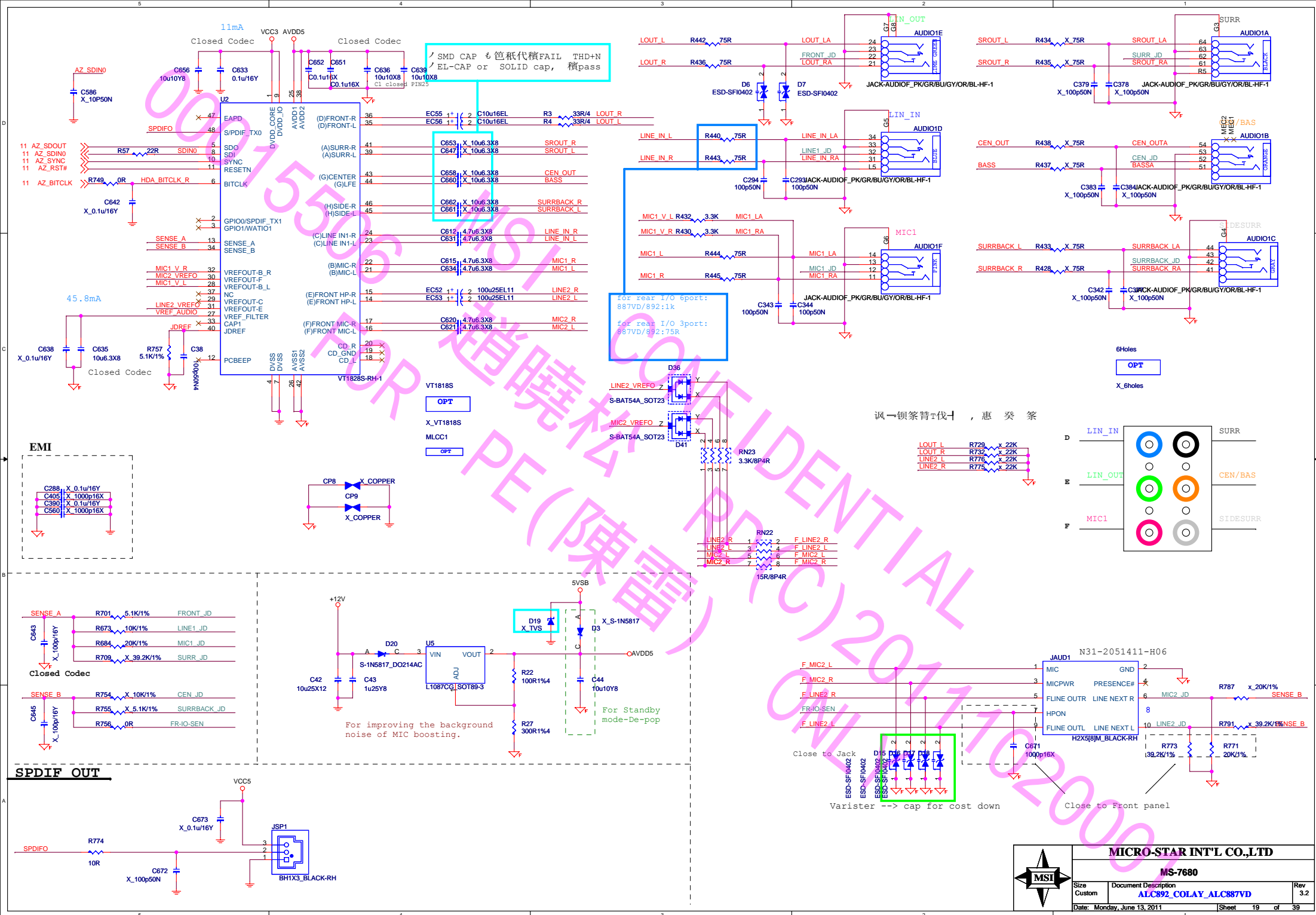
PCI EXPRESS x1-PORT



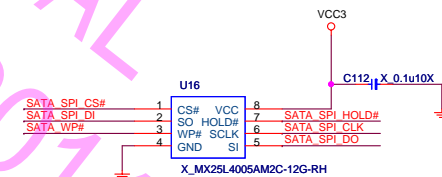
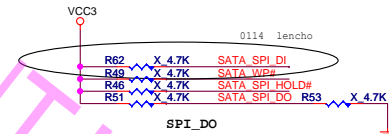
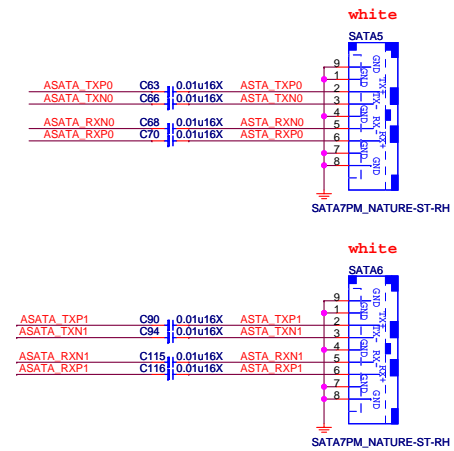
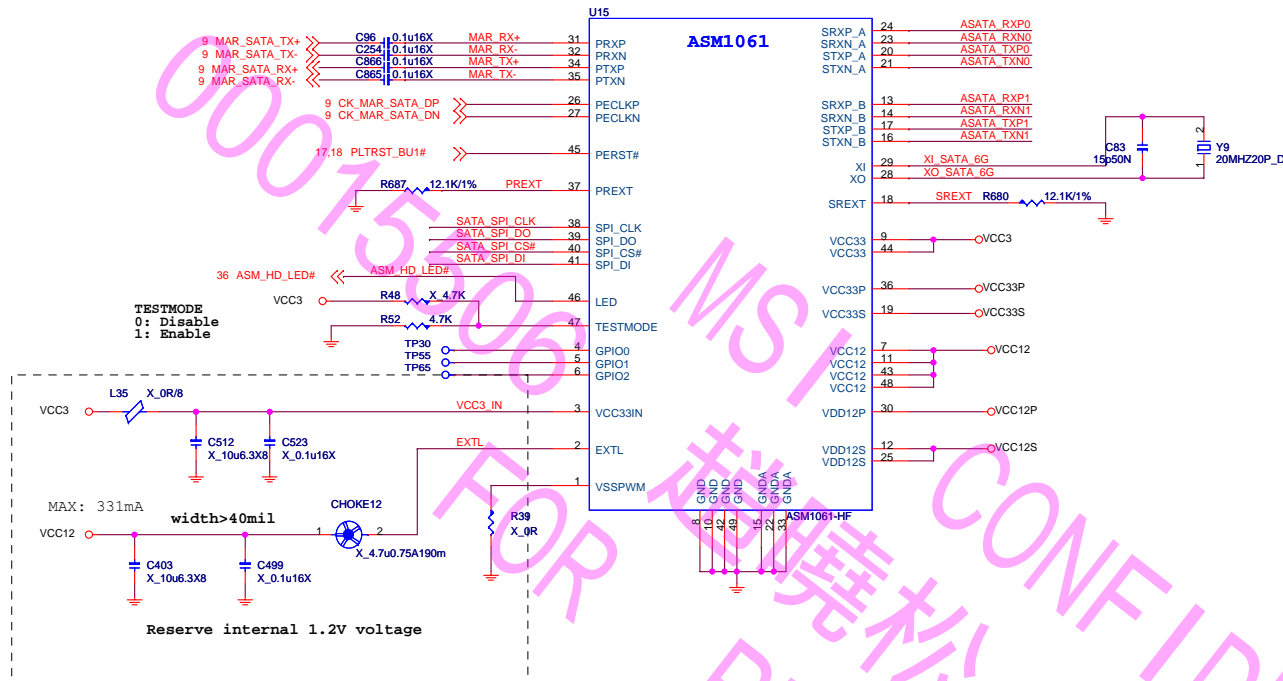
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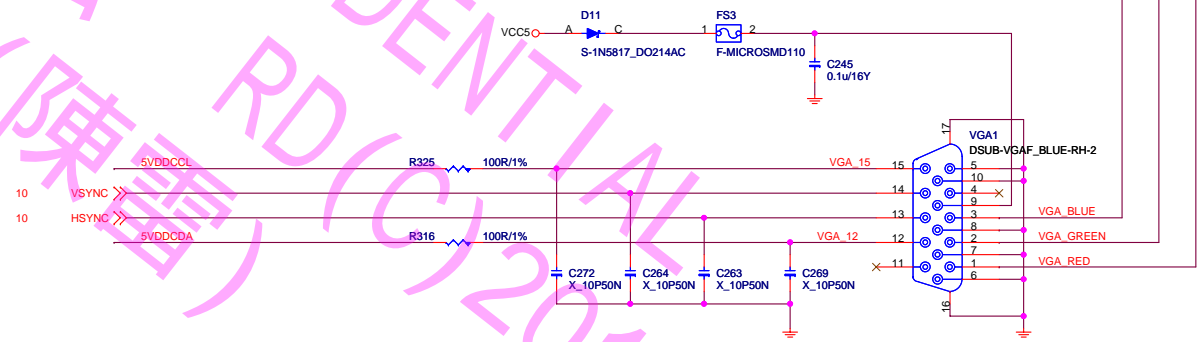
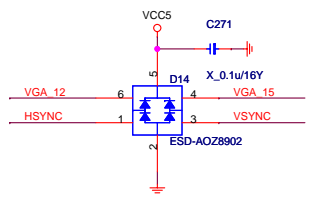
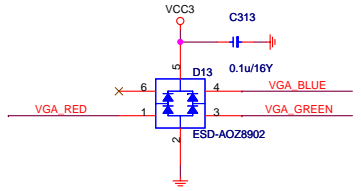
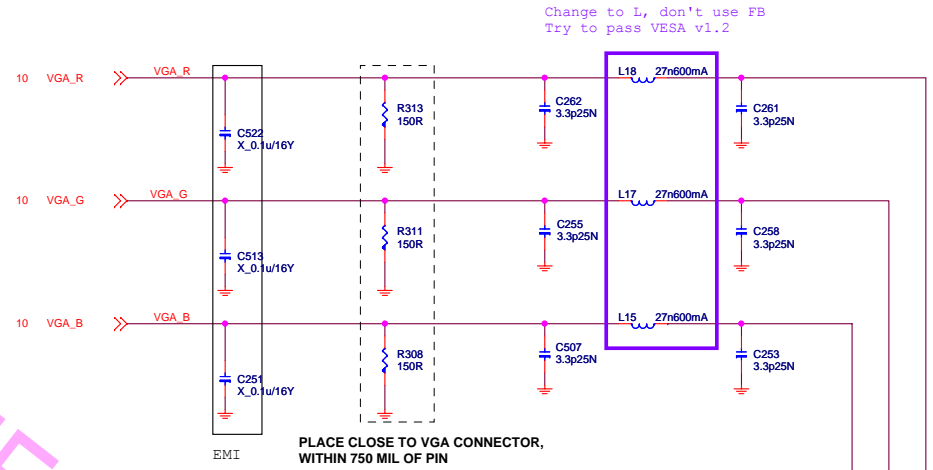
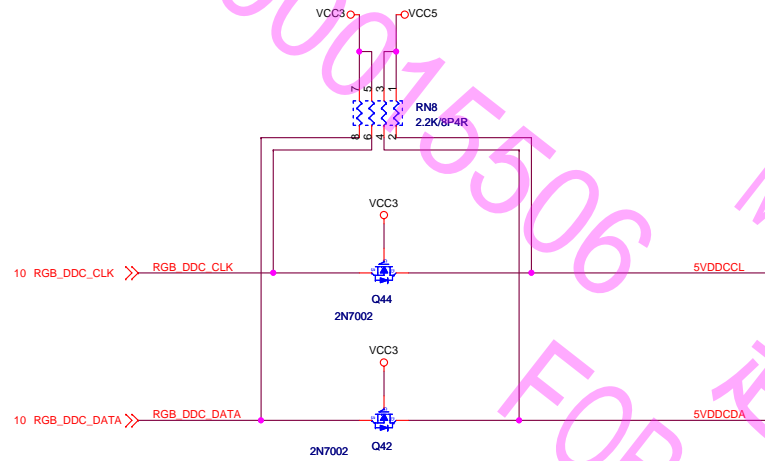
ASM1061 SATA6G



D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

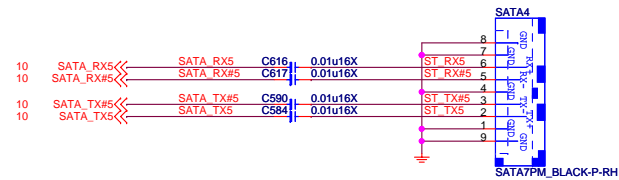
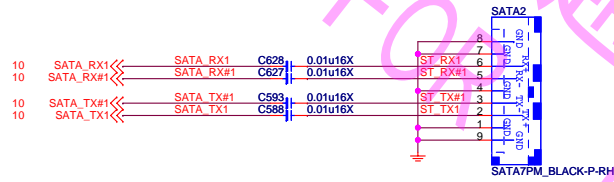
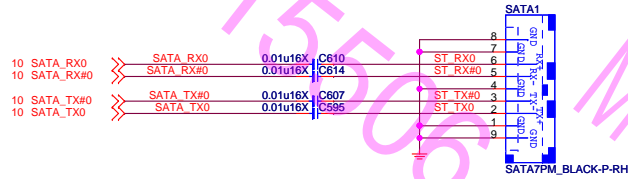
LevelShift



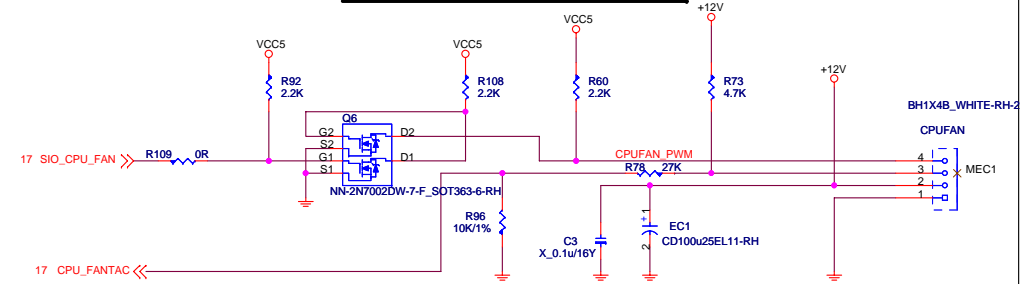
SATA 6G PORT 0,1

H61 PORT 0/1 3G

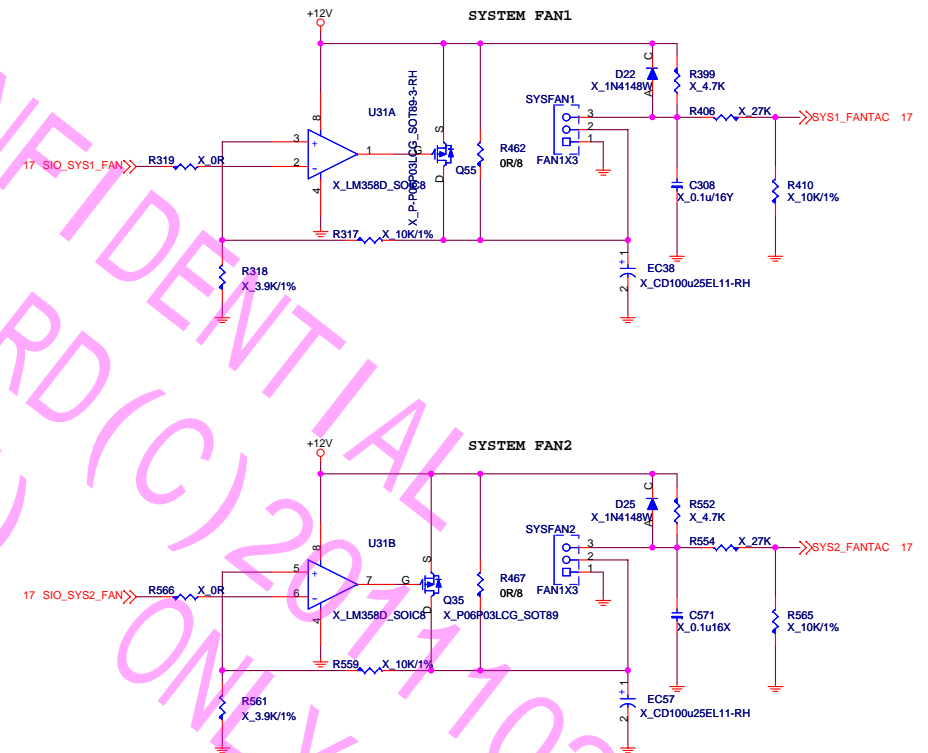
H67 PORT 0/1 6G



CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT

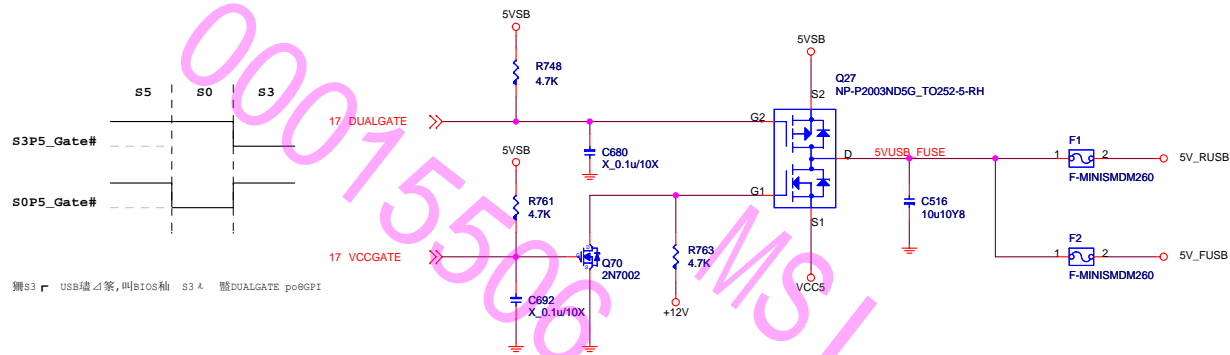


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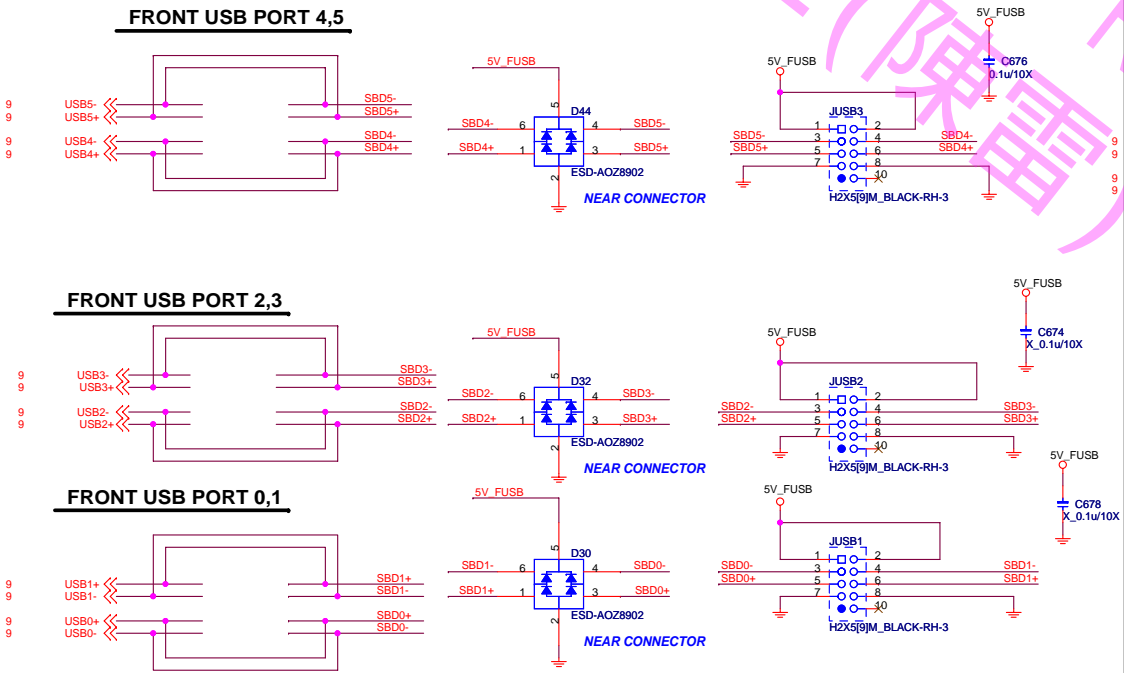
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5V_RUSB Switch



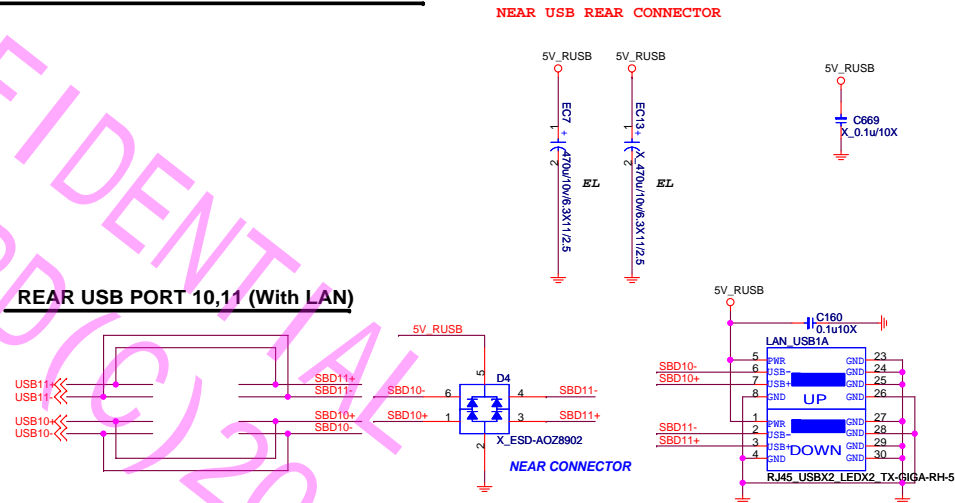
Front USB Connector

For H61 6,7,12,13 Port should be remove

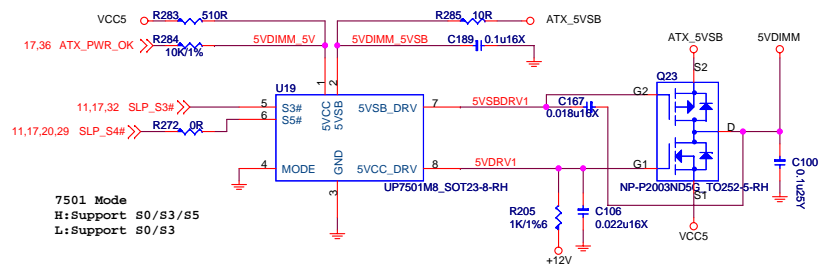


Rear USB Connector

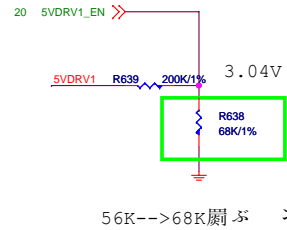
REAR USB PORT 10,11 (With LAN)



5VDIMM FOR DDR



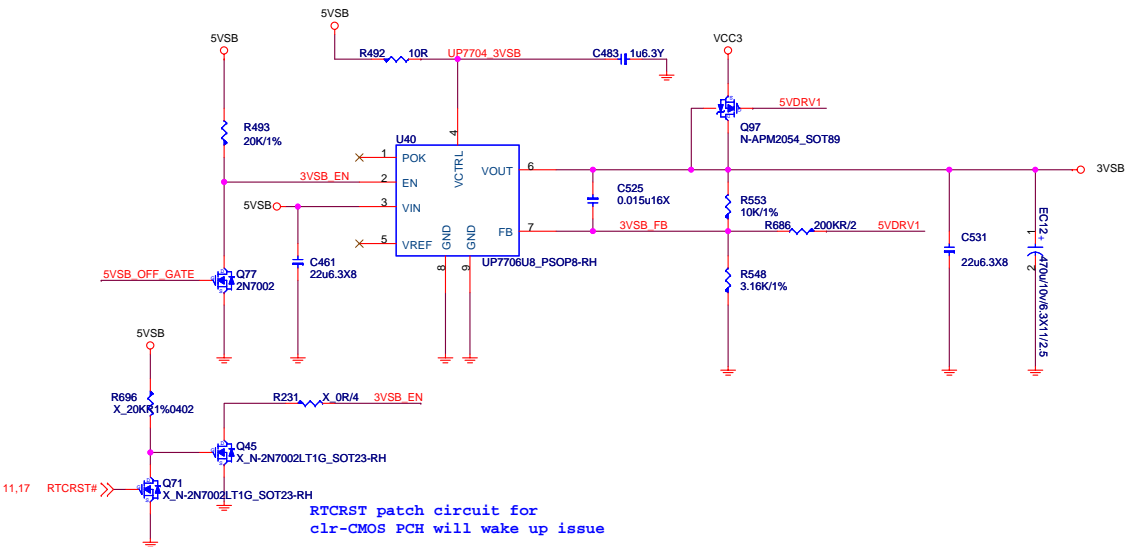
USB MODE



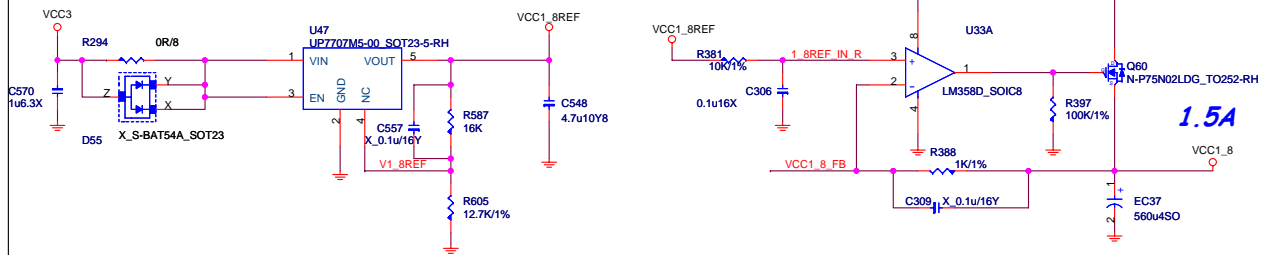
Patch coolermaster 700w power sequence

3VSB

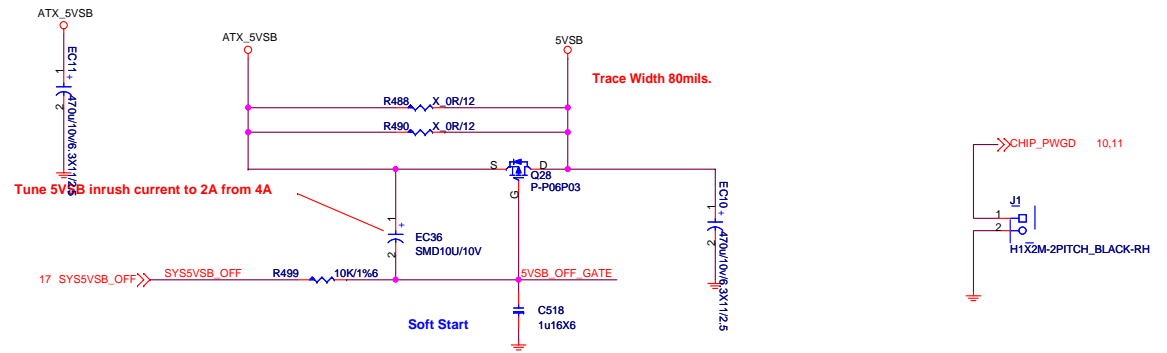
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



VCC1 8REF



5VSB Power Switch

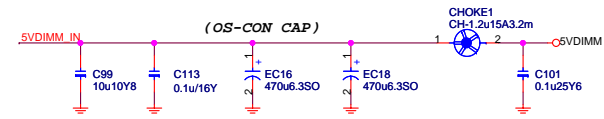
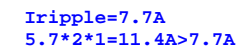


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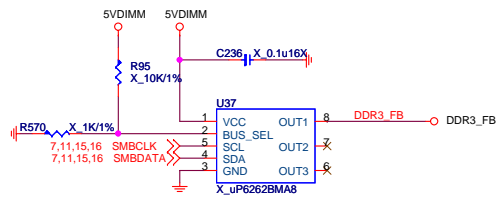
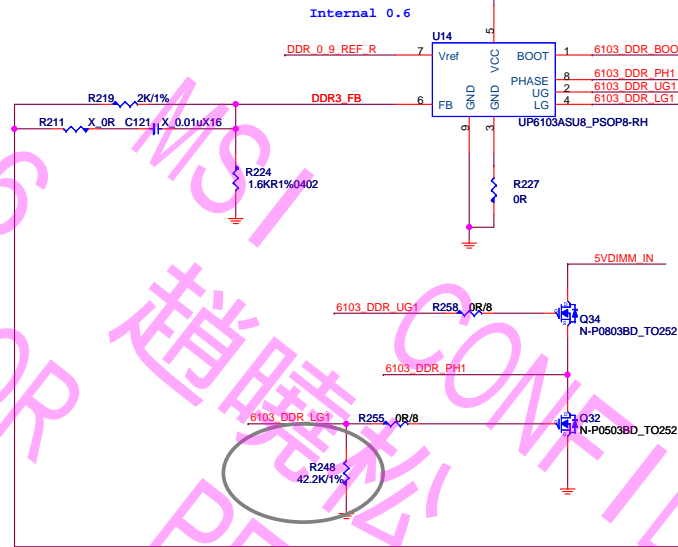
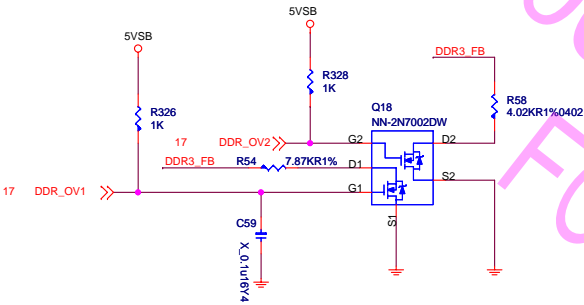
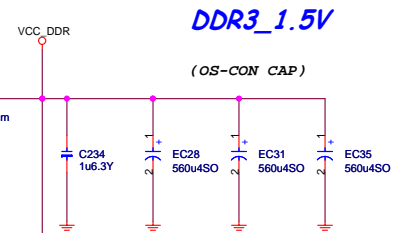
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Size Custom	Document Description ACPI controller UPI	Rev 3.2
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4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT



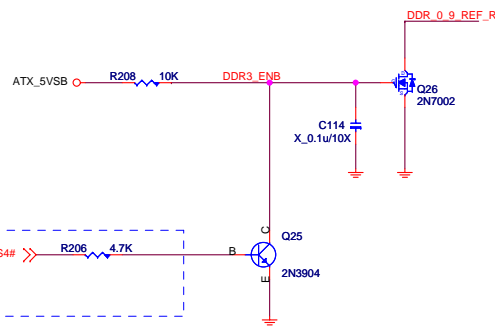
DDR3_1.5V



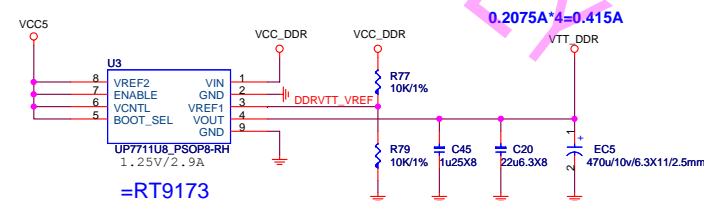
0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

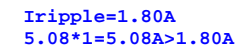


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Size Custom	Document Description DDR Power - uP6103 1-Phase	Rev 3.2
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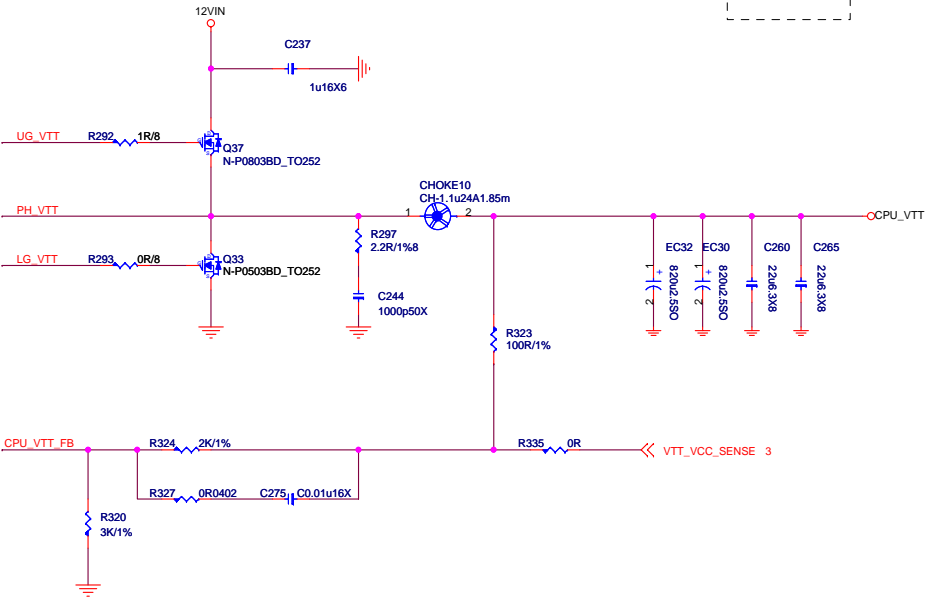
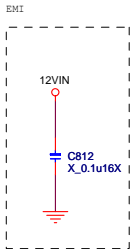
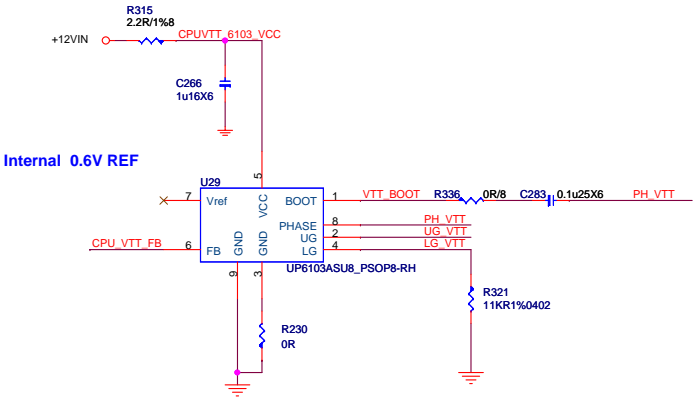
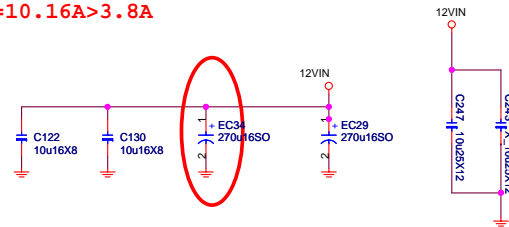
1.8A FOR ME CORE



CPU_VTT:1.05/1.00

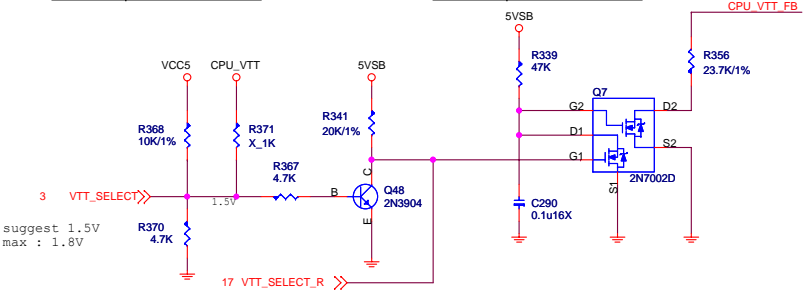
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



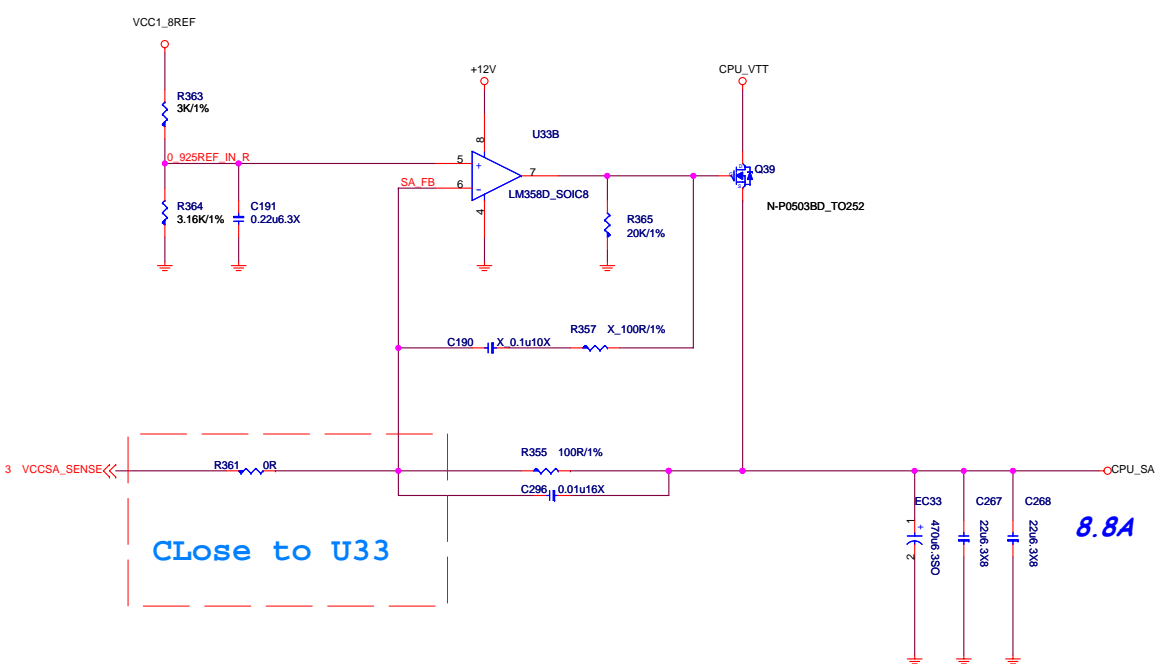
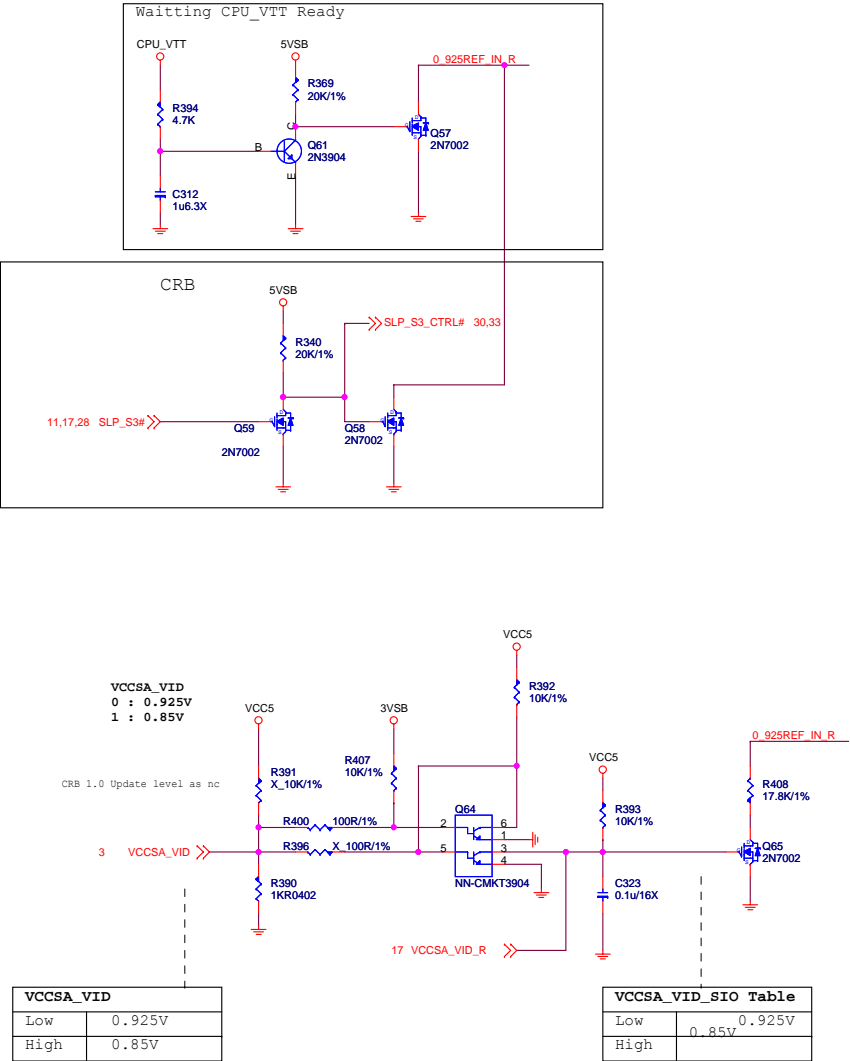
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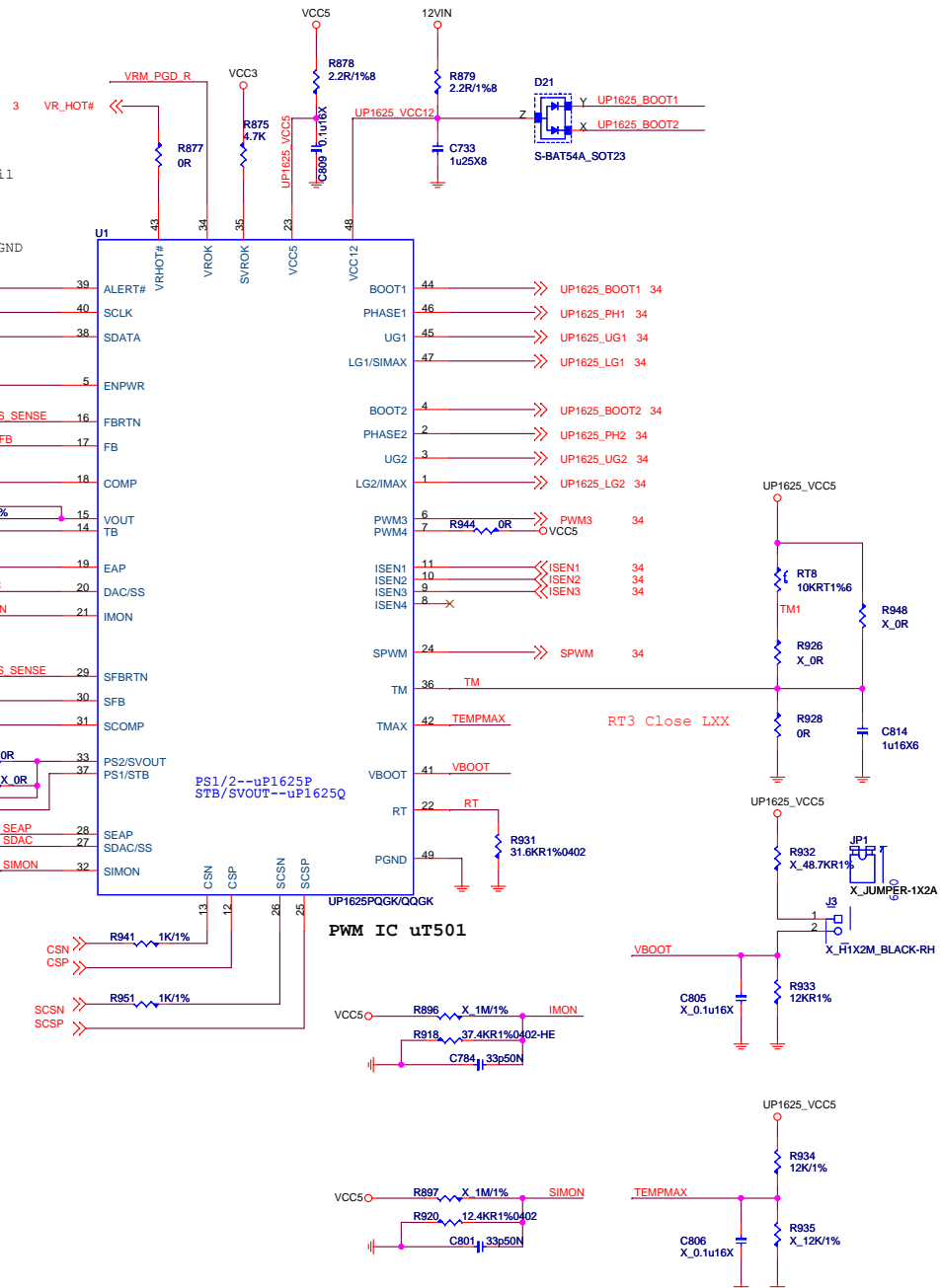
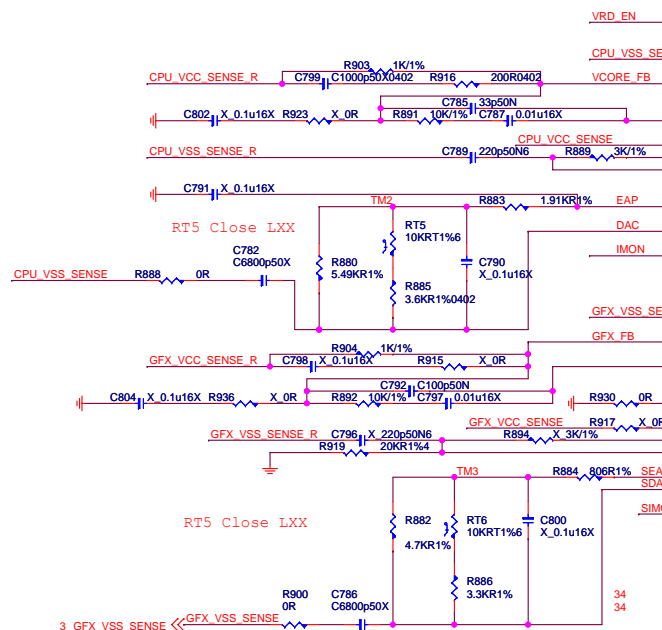
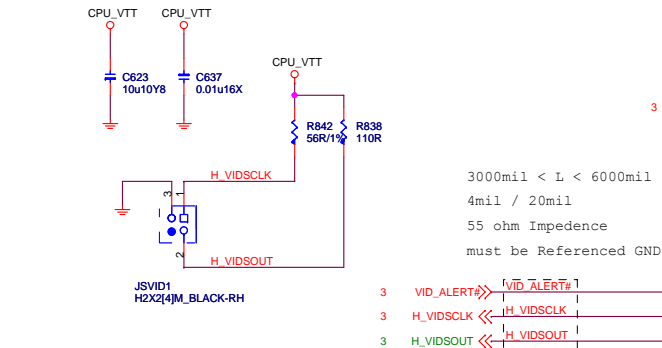
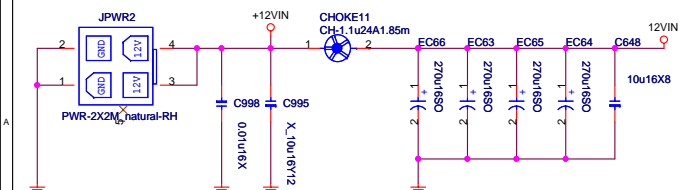
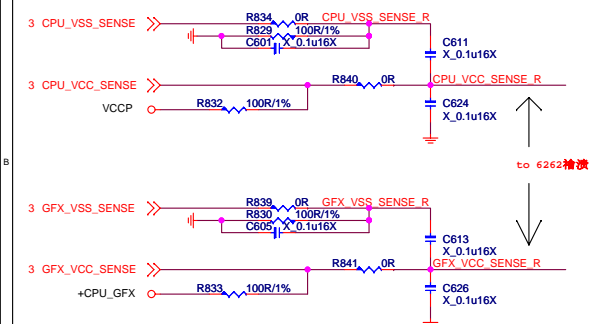
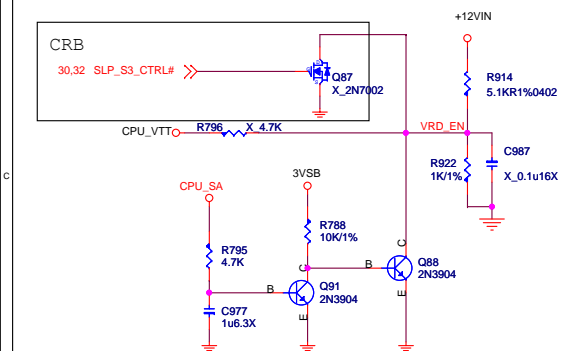
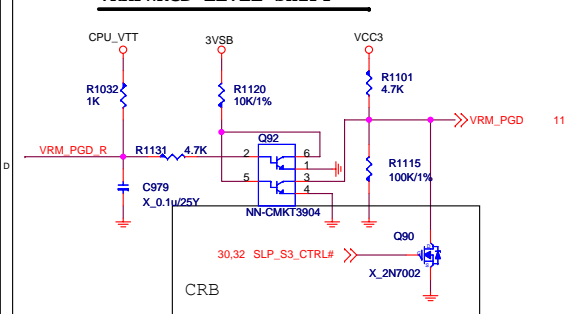
Size	Document Description	Rev
Custom	CPU_VTT - uP6103- 1-Phase	3.2
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CPU_SA:0.925/0.85

SA Core =8.8A



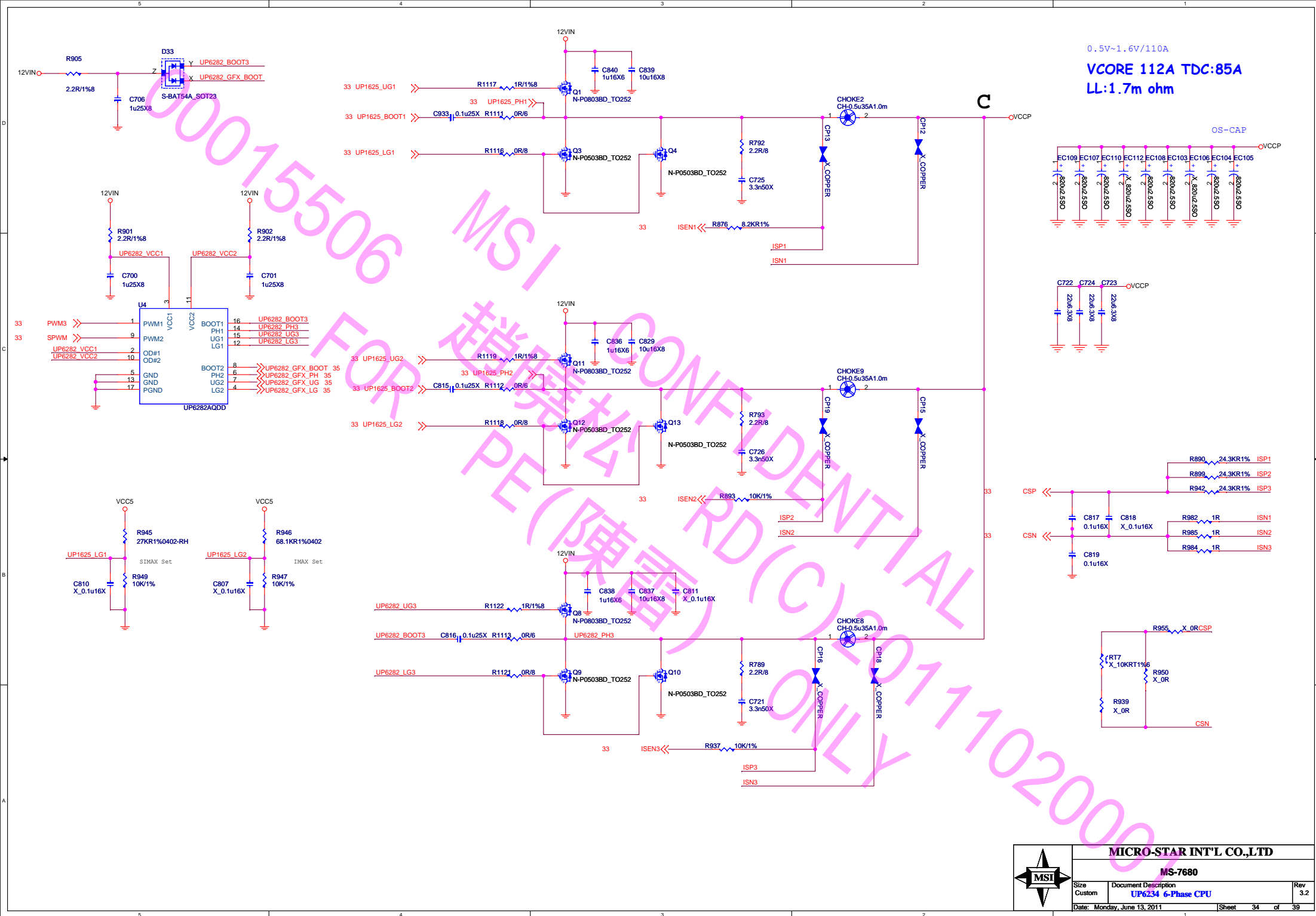
VRMPWRGD LEVEL SHIFT

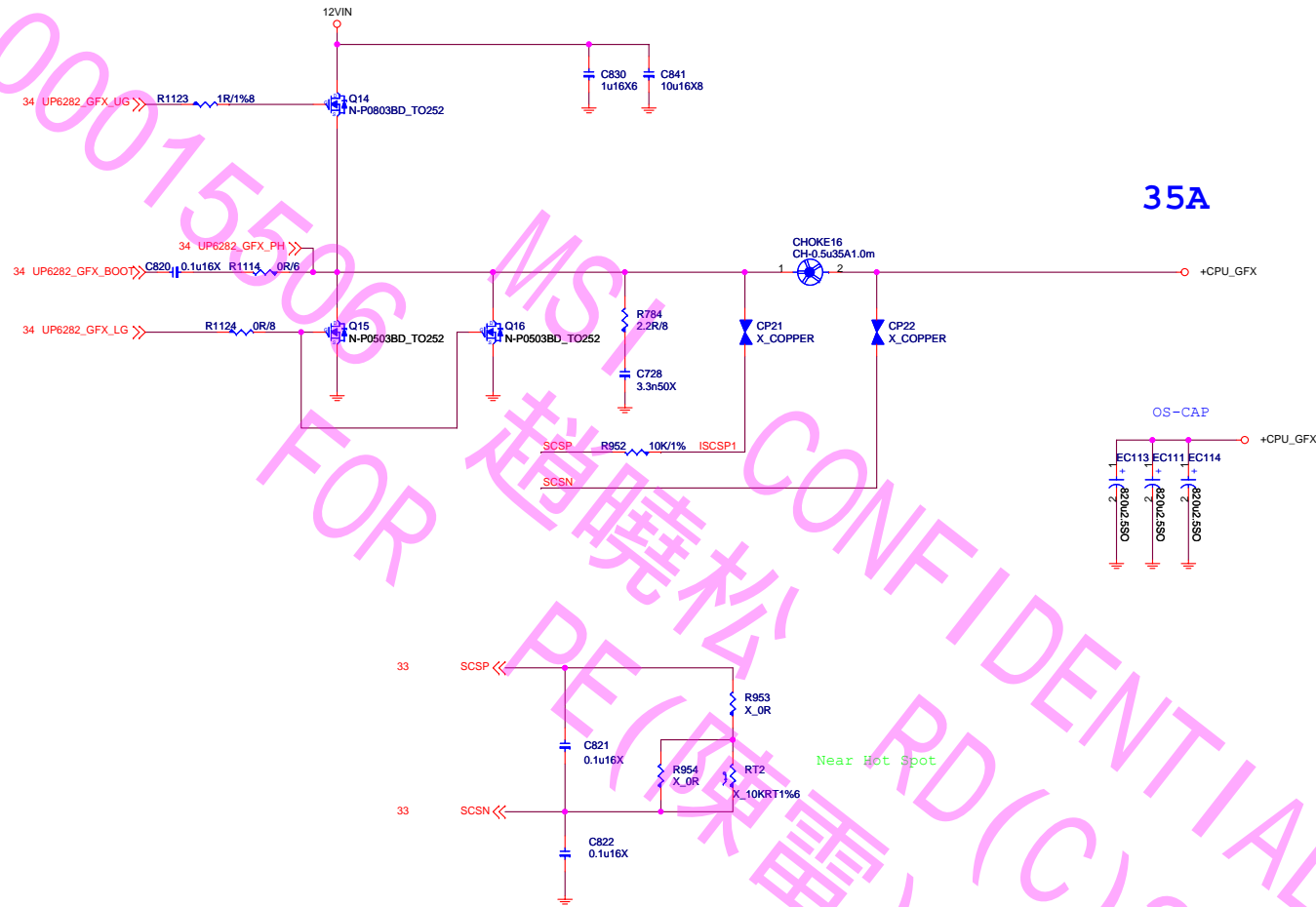


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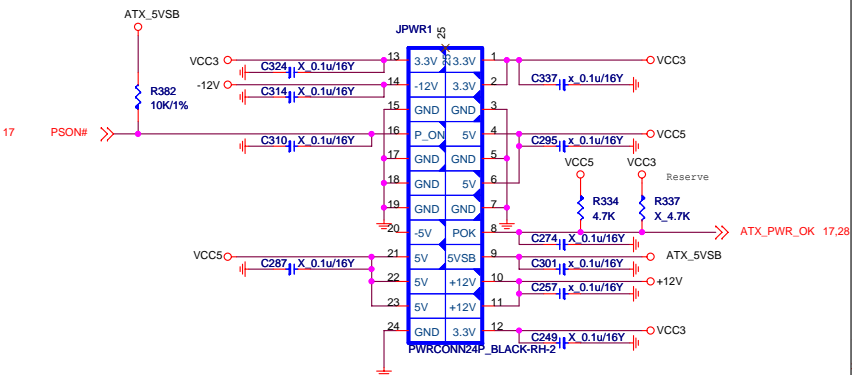
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Size Custom	Document Description VRD12 - UPI6234 6+1-Phase	Rev 3.2
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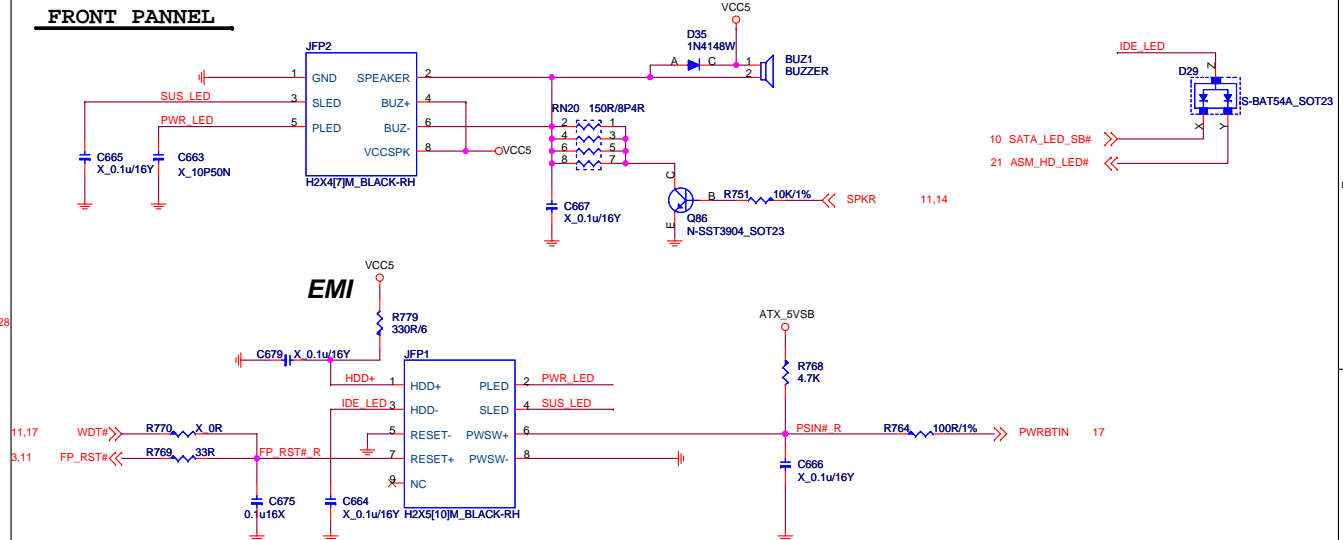




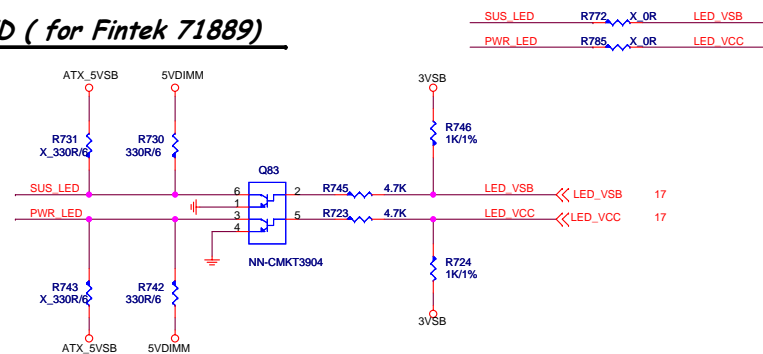
ATX POWER CONNECTOR



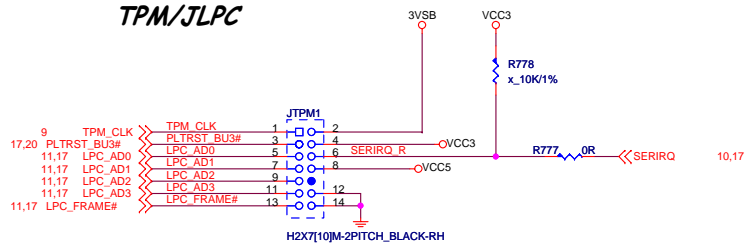
FRONT PANNEL



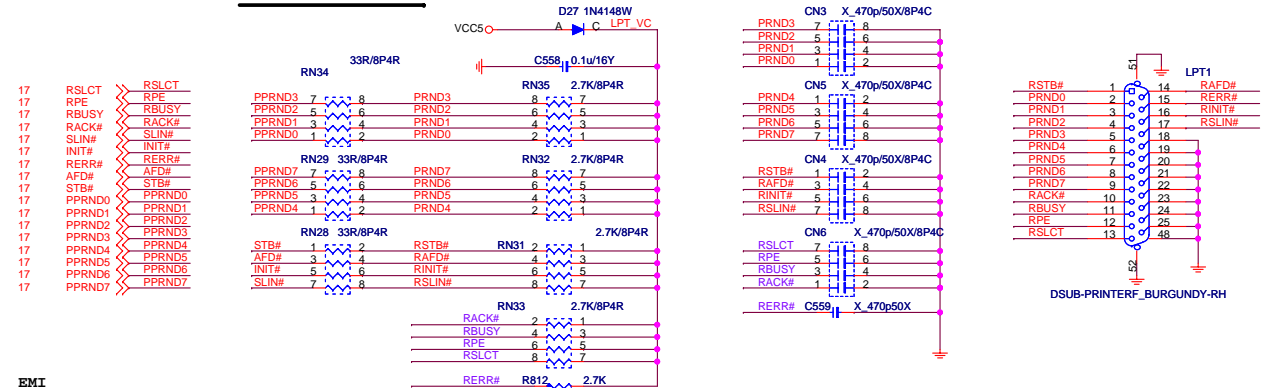
LED (for Fintek 71889)



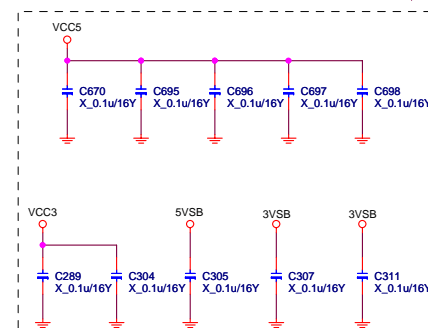
TPM/JLPC



PARALLAL PORT



EMI



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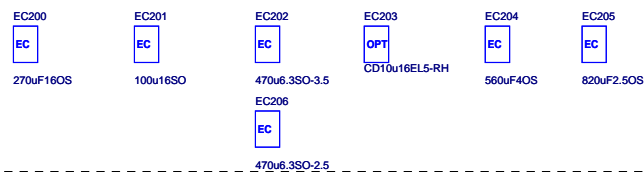
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Size Custom	Document Description ATX PWR-Connector & Front Panel & EMI	Rev 3.2
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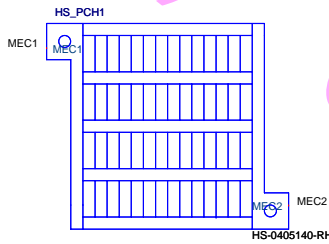
PCH XDP PWRGD/RESET

3IN1
OPT

EL/OS OPT.



Label
OPT



H61M-P21
OPT

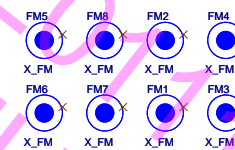
H61M-P23
OPT

H61M-P32
OPT

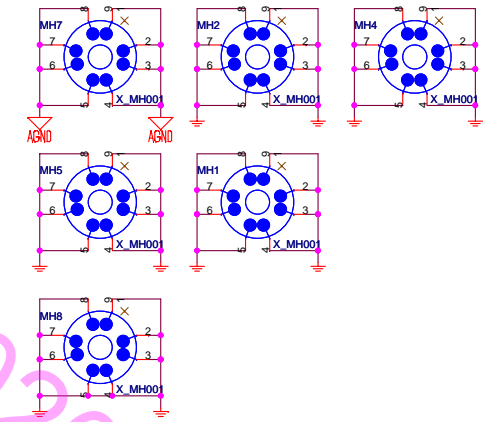
Simulation



Optical Fiducial Marks-120



Mounting Holes



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Custom	XDP / Manual Parts	3.2	
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